



**ESDA5V3L thru
 ESDA25L**

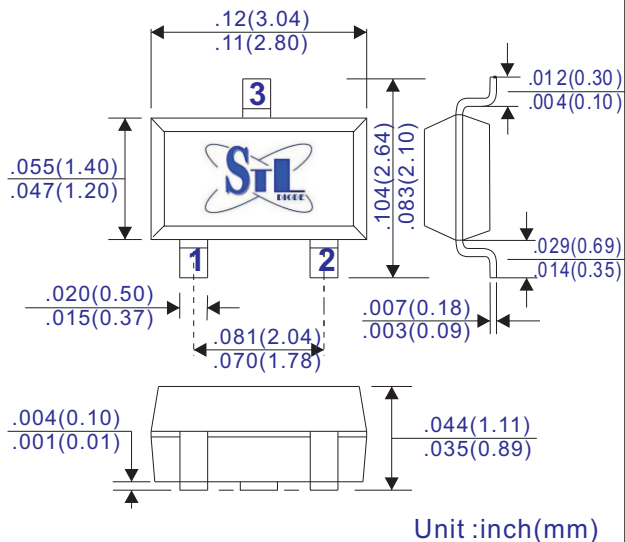
**Dual SMD Transient Voltage
 Suppressor - 5.3V to 25V**



FEATURES & MECHANICAL DATA

- 2 uni-directional or one bi-directional transient suppressor
- Low leakage current: $I_{R\ max.} < 20\mu A$ at V_{BR}
- 300W peak pulse power (8/20 μ S)
- Dual monolithic voltage suppressor designed to protect components which are connected to data & transmission lines against ESD.
- Transient protection for data lines to IEC 61000-4-2 (ESD) 16KV(air), 9KV(contact)
 IEC 61000-4-4 (EFT) 40A (tp=5/50nS)
 MIL STD 883C-Method 3015-6-3 25KV
- Clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for positive transients
- up to 25KV protection level
- Case: Molded plastic SOT-23
- Epoxy: UL94-V0 rated flame retardant
- Mounting Position: Any
- Weight: 0.008 grams (approximate)

SOT-23

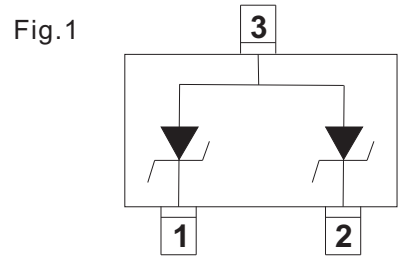


APPLICATIONS

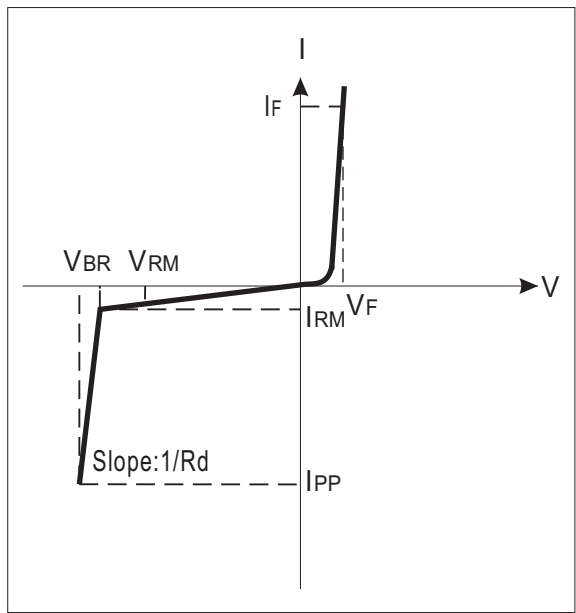
Where transient overvoltage protection in ESD sensitive equipments is required, such as

- COMPUTER
- PRINTER
- COMMUNICATION SYSTEMS

It is particularly recommended for the Rs232 I/O port protection where the line interface withstands only with 2kV ESD surges.



Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{CL}	Clamping Voltage
I_{RM}	Leakage Current
I_{PP}	Peak Pulse Current
αT	Voltage Temperature Coefficient
C	Capacitance
R_d	Dynamic Resistance
V_F	Forward Voltage Drop



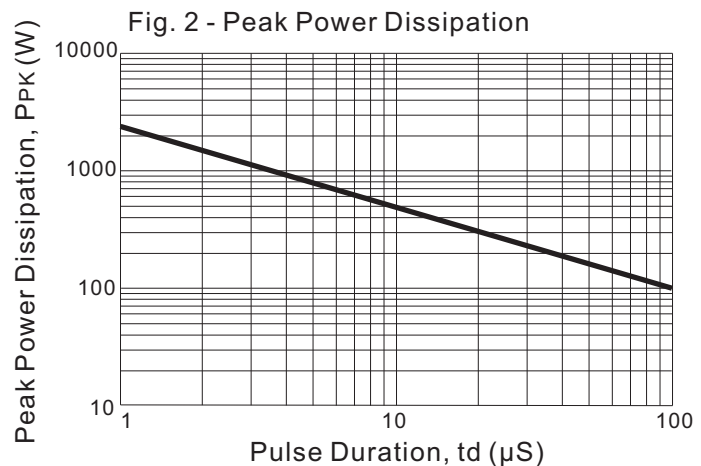
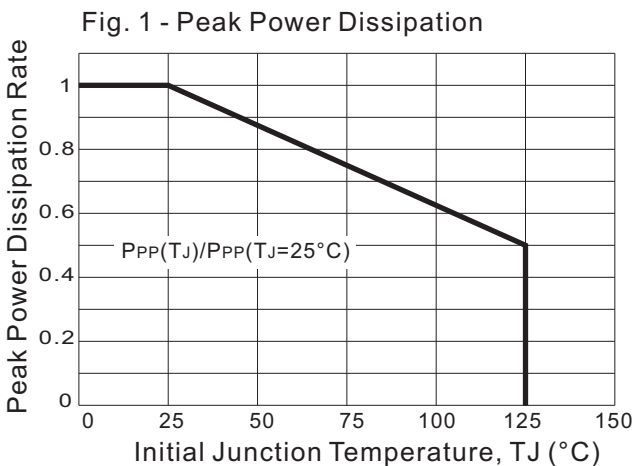


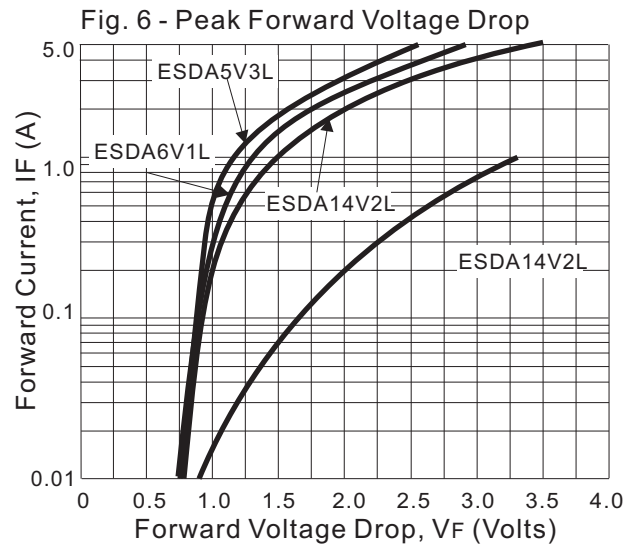
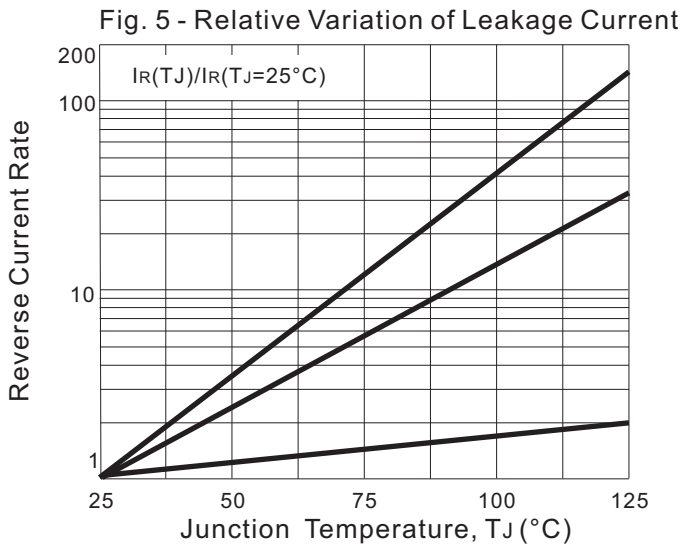
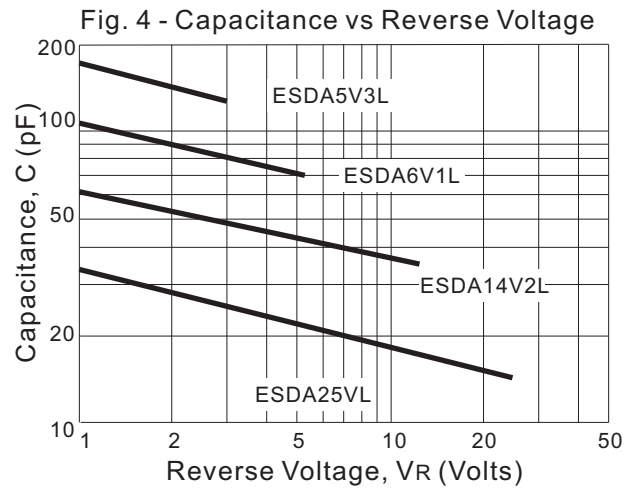
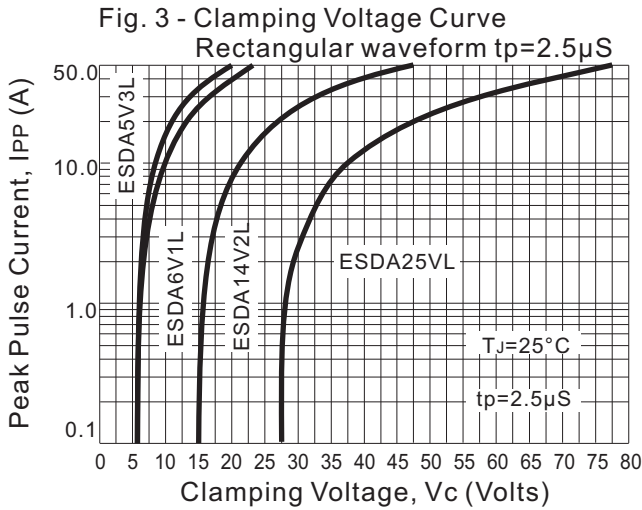
**ESDA5V3L thru
 ESDA25L**

MAXIMUM RATING AND ELECTRICAL CHARACTERISTICS
 Ratings at 25°C ambient temperature unless otherwise specified

	Symbols	ESDA 5V3L	ESDA 6V1L	ESDA 14V2L	ESDA 25L	Units
Minimum Breakdown Voltage @IR=1.0mA min. max.	VBR	5.3 5.9	6.1 7.2	14.2 15.8	25 30	Volts
Stand-off Voltage	VRM	3	5.25	12	24	Volts
Maximum Leakage Current	IRM	2	20	5	1	µA
Electrostatic Discharge MIL STD 883C - Method 3015-6 IEC61000-4-2 Air Discharge IEC61000-4-2 Contact Discharge	-	25 16 9				KV
Peak Pulse Power	PPP	300				Watts
Dynamic Resistance, Note 1	Rd	280	350	650	1000	mΩ
Voltage Temperature Coefficient, Note 2	αT	5	6	10	10	10 ⁻⁴ /°C
Capacitance @VR=0V,f=1.0MHz	C	220	140	90	50	pF
Forward Current	IF	200	200	200	10	mA
Forward Voltage	VF	1.25	1.25	1.25	1.2	Volts
Maximum Junction Temperature	TJ	150				°C
Storage Temperature Range	TSTG	-55 ~ +150				°C
Operation Temperature Range	TOP	-55 ~ +125				°C

Note 1. Square pulse Ipp=15A, tp=2.5µS
 2. VBR=αT x (TA-25°C) x VBR (25°C)





CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage VCL.

This is why we have the dynamic resistance in addition to the classical parameters, The voltage across the protection cell be calculated with the following formula:

$$V_{CL} = V_{BR} + R_d \times I_{PP}$$

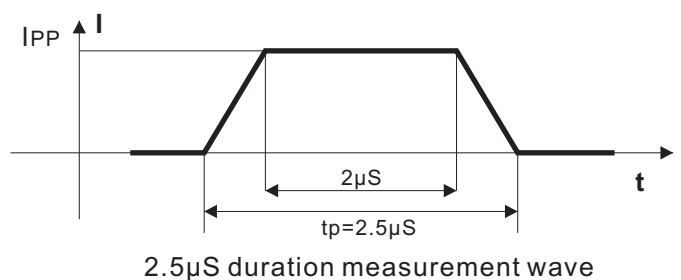
Where IPP is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer

a more adapted test wave, as below defined, to the classical 8/20µS and 10/1000µS surges.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µS, the 2.5µS rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.



1. ESD PROTECTION BY THE ESDAXXL

Electrostatic discharge (ESD) is a major of failure in electronic systems.

Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

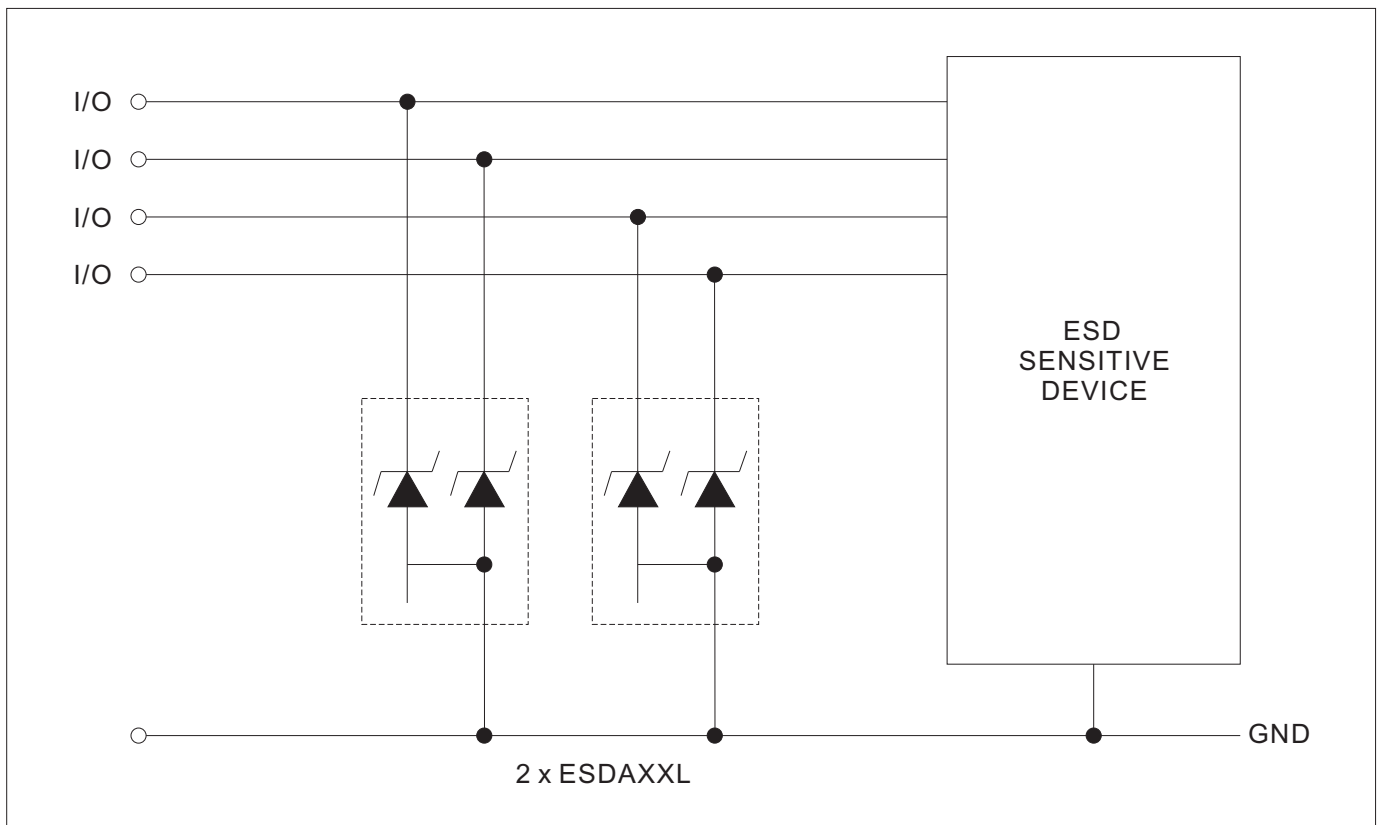
Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements,

connected between the signal line to ground as the transient rises above the operating voltage of the device. the TVS array becomes a low impedance path diverting the transient current to ground.

The ESDAXXL array is the ideal board level protection of ESD sensitive semiconductor components.

The tiny SOT-23 package allows design flexibility in the design of high density boards where the space saving is at a premium. This enables to shorten the routing and contributes to hardening against ESD.



2. CIRCUIT BOARD LAYOUT

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended:

- The ESDAXXL should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.

- All conductive loops, including power and ground loops should be minimized
- The ESD transient return path to ground should be kept as short as possible
- Ground planes should be used whenever possible.